

In the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

1        1.    (Original) A method of performing a dot product operation  
2    with rounding and shifting in a microprocessor in response to a  
3    single rounding dot product instruction, the method comprising the  
4    steps of:  
5        fetching a first pair of elements and a second pair of  
6    elements;  
7        forming a first product of the first pair of elements and a  
8    second product of the second pair of elements;  
9        combining the first product with the second product to form a  
10 combined product;  
11       rounding the combined product to form an intermediate result;  
12 and  
13       shifting the intermediate result a selected amount to form a  
14 final result.

2.    (Canceled)

1       3.    (Currently Amended) The method of Claim ~~2~~ 1, wherein the  
2    step of rounding adds a rounding value to the combined product via  
3    an arithmetic circuit having a first input receiving said first  
4    product, a second input receiving said second product and a carry  
5    input to a mid-position receiving said rounding value to form the  
6    intermediate result, and wherein the step of shifting shifts the  
7    intermediate result right by a selected shift amount.

1       4.    (Currently Amended) The method of Claim 3, wherein the  
2    rounding value is ~~2\*\*n~~ 2<sup>n</sup> and the selected shift amount is n+1.

1           5.    (Original) The method of Claim 4, wherein n has a fixed  
2   value of fifteen.

Claims 6 to 8. (Canceled)

1           9.    (Original) The method of Claim 1, wherein the step of  
2   forming treats a one of the first pair of elements as a signed  
3   number value and treats another one of the first pair of elements ✓  
4   as an unsigned number value.

1           10. (Original) The method of Claim 1, wherein the step of  
2   combining comprises subtracting the product of second pair of ✕  
3   elements from the product of first pair of elements.

1           11. (Original) The method of Claim 1, wherein the step of  
2   combining comprises adding the product of second pair of elements ✕  
3   to the product of first pair of elements.

B1  
12. (Canceled)

1           13. (Original) A digital system having a microprocessor  
2   operable to execute a rounding dot product instruction, wherein the  
3   microprocessor comprises:  
4       storage circuitry for holding pairs of elements;  
5       a multiply circuit connected to receive a first number of  
6   pairs of elements from the storage circuitry in a first execution  
7   phase of the microprocessor responsive to the dot product  
8   instruction, the multiply circuit comprising a plurality of  
9   multipliers equal to the first number of pairs of elements;  
10       an arithmetic circuit connected to receive a plurality of  
11   products from the plurality of multipliers, the arithmetic circuit  
12   having a provision for mid-position rounding responsive to the

13 rounding dot product instruction; and  
14 a shifter connected to receive an output of the arithmetic  
15 circuit, the shifter operable to shift a selected amount in  
16 response to the rounding dot product instructions.

1 14. (Original) The digital system of Claim 13, wherein the  
2 arithmetic circuit has a carry input connected to a mid-position,  
3 wherein the carry input is asserted in response to the rounding dot  
4 product instruction.

B1 1 15. (Original) The digital system according to Claim 1 being X  
2 a cellular telephone, further comprising:  
3 an integrated keyboard connected to the processor via a  
4 keyboard adapter;  
5 a display, connected to the processor via a display adapter;  
6 radio frequency (RF) circuitry connected to the processor; and  
7 an aerial connected to the RF circuitry.

1 16. (New) The method of Claim 3, wherein:  
2 the step of shifting sign extends the intermediate result. 112

1 17. (New) The digital system of Claim 13, wherein:  
2 the shifter right shifts and sign extends the output of the  
3 arithmetic circuit.

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